AF

[10191/821]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

Inventors	:	Holger BELLMANN et al.
Serial No.	:	09/166.496
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For	:	CONTROL DEVICE FOR A SYSTEM, AND METHOD FOR OPERATING THE CONTROL DEVICE
Group Art Unit	:	3661
Examiner	:	Brian J. BROADHEAD
Confirmation No.	:	9214

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Signature:
Jong H. Lee

APPELLANTS' REPLY BRIEF
UNDER 37 C.F.R. § 41.41

S I R :

In response to the Examiner's Answer mailed on May 21, 2007, Applicants submit this Reply Brief in support of their appeal.

ARGUMENTS

Claims 1, 3, 12 and 14 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 4,642,756 ("Sherrod"). Applicants respectfully submit that the Sherrod reference does not anticipate claims 1, 3, 12 and 14 for at least the following reasons.

To anticipate a claim under 35 U.S.C. § 102(b), the Office must demonstrate that each and every claim limitation is *identically disclosed* in a single prior art reference. (See Scripps Clinic & Research Foundation v. Genentech, Inc., 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991)). "The identical invention must be shown in as complete detail as is contained in the claim." M.P.E.P. § 2131. If any claimed element is absent from a prior art reference, it cannot anticipate the claim. See Rowe v. Dror, 112 F.3d 473, 478 (Fed. Cir. 1997). To the extent that the Examiner may be relying on the doctrine of inherent disclosure to support the anticipation rejection, the Examiner must provide a "basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristics necessarily flow from the teachings of the applied art." (See M.P.E.P. § 2112; emphasis in original; see also Ex parte Levy, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990)).

Independent claim 1 recites, in relevant parts, the following: "A control device for controlling a system, comprising . . . ***a scheduler*** activating the activatable modules as a function of the respective corresponding priority value of each of the activatable modules to provide activated modules, ***the activated modules generating data by analyzing states of the system***; and ***a priority manager*** continuously modifying the respective corresponding priority value of each of at least one of the activatable modules individually to one of increase and decrease the respective corresponding priority value relative to the priority value of another of the activatable modules." Independent claim 12 recites method limitations corresponding to the above-recited device limitations of claim 1.

In support of the rejection, the Examiner asserted in the final Office Action that col. 4, lines 1 to 8, of the Sherrod reference disclose a plurality of activatable modules with corresponding priority values. However, as Applicants noted in the Appeal Brief, col. 4, lines 1-8 of Sherrod merely indicate that storage and I/O peripherals 3', as well as user interactive terminal display 4', are connected to CPU 5', thereby allowing the computer system to access storage

devices and "communicate with the outside world." Clearly nothing in this passage of the Sherrod reference suggests the claimed feature of "***the activated modules generating data by analyzing states of the system,***" as recited in claims 1 and 12. In order to overcome this glaring deficiency, the Examiner now contends in the Examiner's Answer the following: a) "**the tasks** disclosed in Sherrod [col. 3, l. 14-18 & 35-37; col. 4, l. 35-40] are equivalent to the **activatable modules**"; b) the claimed limitation of "***the activated modules generating data by analyzing states of the system***" has been "**given a very broad interpretation**"; and c) "[s]ince the tasks disclosed in Sherrod are performing I/O operations . . . , it is very clear that the modules are generating data by analyzing the states of the system," i.e., "for any I/O operation, **inputs are the states of the system** and the outputs are the generated data." Applicants respectfully submit that the Examiner's assertions are factually and legally incorrect, as explained in detail below.

To the extent the Examiner summarily states that the claimed limitation of "***the activated modules generating data by analyzing states of the system***" has been "**given a very broad interpretation**," it is a fundamental rule of claim interpretation that the Examiner cannot unilaterally give "**a very broad interpretation**"; instead, claims should be given "the broadest **reasonable** interpretation" **that is consistent with the specification and the interpretation that those skilled in the art would reach**. (See M.P.E.P. 2111, citing In re Hyatt, 211 F.3d 1367 (Fed. Cir. 2000), and In re Cortright, 165 F.3d 1353 (Fed. Cir. 1999)). In this regard, the Examiner has provided absolutely no basis for making the asserted "**very broad interpretation**." To the extent the Examiner states that "for any I/O operation, **inputs are the states of the system** and the outputs are the generated data," this assertion assumes an existence of a "system" that is not clearly identified by the Examiner. What exactly is the alleged "system" and the corresponding "states of the system" allegedly suggested by Sherrod? The Examiner has previously stated that the claimed limitation of "***the activated modules generating data by analyzing states of the system***" is "disclosed in Sherrod as the tasks themselves," i.e., "[e]ach task of the system is doing some action that depends on the state of the system." (3/1/06 Final Office Action, p. 3-4). To the extent the Examiner may be contending that the computer system or the task of Sherrod is the equivalent of the claimed "system" recited in claim 1, this interpretation is clearly contrary to the Applicants' specification and the interpretation that those skilled in the art would reach. The present specification (e.g., Fig. 1; p. 2, l. 23-32) clearly indicates the following: a) control device 1 is connected via lines 4 to a separate system 2 to be controlled; b) "control device 1 has a microcomputer 3 which is provided for the execution of [plurality of] modules 10";

c) and examples of the system 2 include a motor vehicle, an internal combustion engine, or a transmission. Clearly, the "control device" includes the computer 3, and the "system" refers to a separate system 2 which is distinct from the computer of the control device. Given this unambiguous disclosure, there is no reasonable basis for the Examiner to contend that the "system" of claim 1 should be interpreted to refer to the computer or the task of the control device, and indeed there is no reasonable basis to contend that the Examiner's interpretation is the interpretation that those skilled in the art would reach. Given the clear conclusion that the "system" of claim 1 refers to a separate system which is distinct from the computer or the task of the control device, the Examiner's assertion that "for any I/O operation, inputs are the states of the system and the outputs are the generated data" is simply irrelevant to the present claimed subject matter, and the Examiner's assertion clearly does not support the conclusion that that the claimed limitation of "***the activated modules generating data by analyzing states of the system***" is taught or suggested in any way by Sherrod.

Independent of the above, with respect to the claimed limitation of "a scheduler activating the activatable modules as a function of the respective corresponding priority value of each of the activatable modules," the Examiner contends in the Examiner's Answer that this feature is taught in col. 3, l. 7-22 and col. 4, l. 11-16 and 24-25 of Sherrod, and the Examiner makes the following additional statements in support: a) "the scheduler is disclosed as being part of the logic circuit 7' in Sherrod"; b) the "logic circuit is disclosed as containing the instructions and data required to carry out its functions (lines 24-25, col. 4)"; c) "[t]he functions carried out are further disclosed as the method described on lines 54-58, on column 5"; and d) "[t]here are two distinct functions disclosed as being part of the method," which "would correspond to two distinct sets of instructions contained on program logic 7'." In addition, the Examiner further contends that the claimed limitation of "a priority manager continuously modifying the respective corresponding priority value of each of at least one of the activatable modules individually to one of increase and decrease the respective corresponding priority value **relative to the priority value of another of the activatable modules**" is somehow taught by one of the two distinct sets of instructions contained on program logic 7'. Applicants respectfully submit that the above-noted assertions made by the Examiner are factually and/or logically incorrect, as explained below.

First, with respect to the Examiner's statement that "the scheduler is disclosed as being part of the logic circuit 7' in Sherrod," this is clearly wrong: Fig. 3 and col. 4, l. 8-9 of

Sherrod clearly indicate that the logic circuit 7' is part of the scheduler 6'. Second, with respect to the Examiner's statement that "logic circuit is disclosed as containing the instructions and data required to carry out its functions (lines 24-25, col. 4)," the cited section actually indicates that "RAM 8' and ROM 9' store the instructions and data required by logic circuit 7'." Third, to the extent the Examiner further contends that the claimed limitation of "**a priority manager continuously modifying** the respective corresponding priority value of each of at least one of the activatable modules individually to one of increase and decrease the respective corresponding priority value **relative to the priority value of another of the activatable modules**" is somehow taught by one of the two distinct sets of instructions contained on program logic 7', there is simply no teaching or suggestion in Sherrod that the **priority value** is changed relative to the **priority value** of another module **by a priority manager**; instead, the Sherrod reference only states that the overall priority sequence of the tasks is based on the combination of internal priority (provided from within the task scheduler 6'; col. 4, l. 31-33) and external priority (assigned by the computer operator or the task itself; col. 4, l. 33-35). To the extent the Examiner continues to assert that "when a priority of one task is changed it is relative to another task," and "this must happen whenever a task priority is changed in Sherrod," this assertion is contradicted by the actual disclosure of Sherrod. With respect to "**external priorities**" discussed in Sherrod (and shown in Table 1), it is clear that **neither "a scheduler" nor "a priority manager" has any influence on changing the external priorities**, since the external priorities are assigned by the computer operator or the task itself. Furthermore, with respect to "**internal priorities**" discussed in Sherrod (and shown in Table 2), the assigned internal priority of a given task depends on the "state" of the task, i.e., a given task may have one of **six different fixed internal priority levels corresponding to different task states**, which means a change in the internal priority value of a given task according to Sherrod does not necessarily result in a change in the priority of the given task relative to the priority of another task. The mere possibility that a change in the internal **priority value** of a given task may result in a change in the priority of the given task relative to the priority of another task does not inherently teach the claimed feature of "**a priority manager modifying** the corresponding **priority value** of at least one of the modules individually to one of increase and decrease the respective corresponding priority value **relative to the priority value of another of the activatable modules**," since there is no "basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristics necessarily flow from the teachings of the applied art." To the extent the Examiner cites the "example on lines 45-47, on column 5" of Sherrod as supporting the contention that "when a priority of one task is

changed it [must be] relative to another task," the cited section does not address **changing** of relative priorities in the overall priority sequence; instead, the cited section merely states the rule for determining the overall priority sequence for two tasks having the same internal and external priority states, based on which task was first assigned the priority states.

For at least the foregoing reasons, claims 1 and 12, as well as their dependent claims 3 and 14, are allowable over Sherrod.

For the foregoing reasons, it is respectfully submitted that the final rejection of claims 1, 3, 12 and 14 should be reversed.

Respectfully submitted,

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